CY-RB4111 FX3 USB3 Vision Solution Demo

CONTENTS

PAGE	DESCRIPTION
01	Title & Table of Contents
02	Block Diagram
03	USB TYPE-C CONNECTOR
04	FX3 POWER
05	FX3- POWER INTERFACE
06	FX3-SIGNALS
07	FPGA-POWER
08	FPGA-SIGNALS
09	FPGA-DDR3 SIGNALS
10	DDR3 SDRAM
11	IT6801FN CIRCUITS
12	FPGA - Image sensor signals
13	FPGA-SERDES
14	Revision History

Drawing Numbers	
PCBA	121-60624-01
PCB	600-60624-01
FAB DRW	610-60624-01
ASSY DRW	620-60624-01
SCH DRW	630-60624-01

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SCH Title : CY-RB4111 FX3 USB3 Vision Solution Demo

Page Title : Title Page

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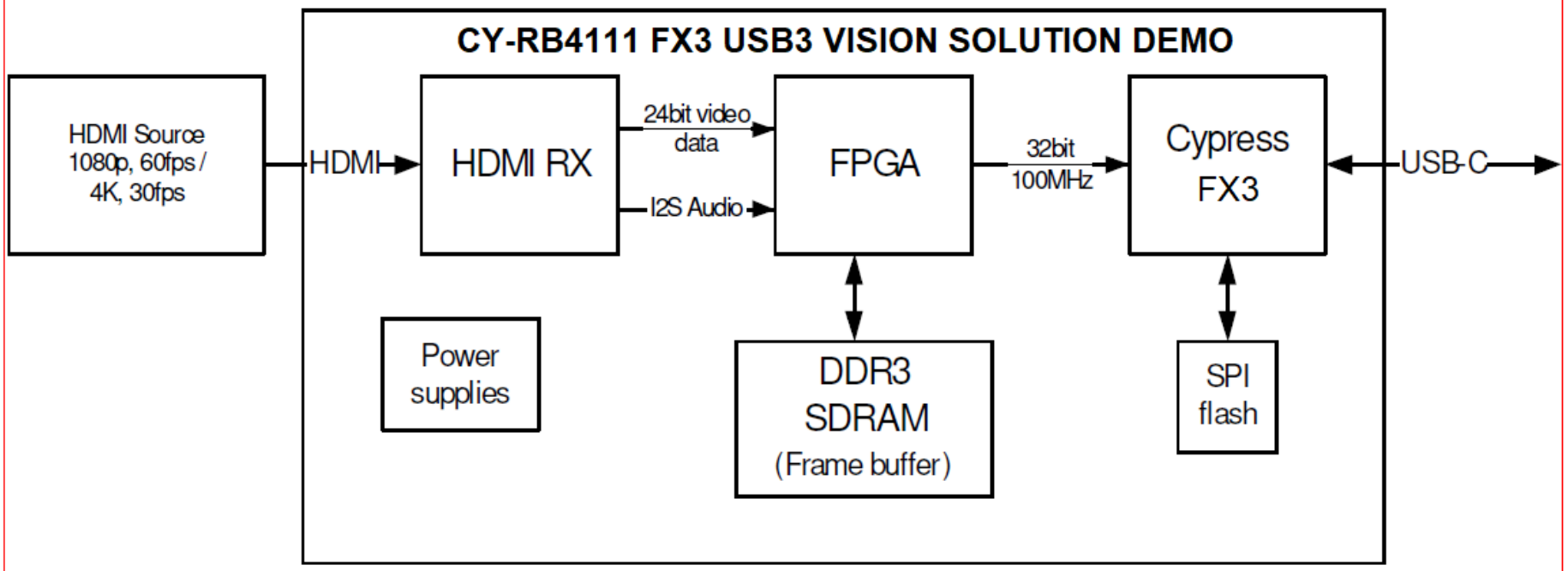

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SCH Title : CY-RB4111 FX3 USB3 Vision Solution Demo

Page Title : Block diagram

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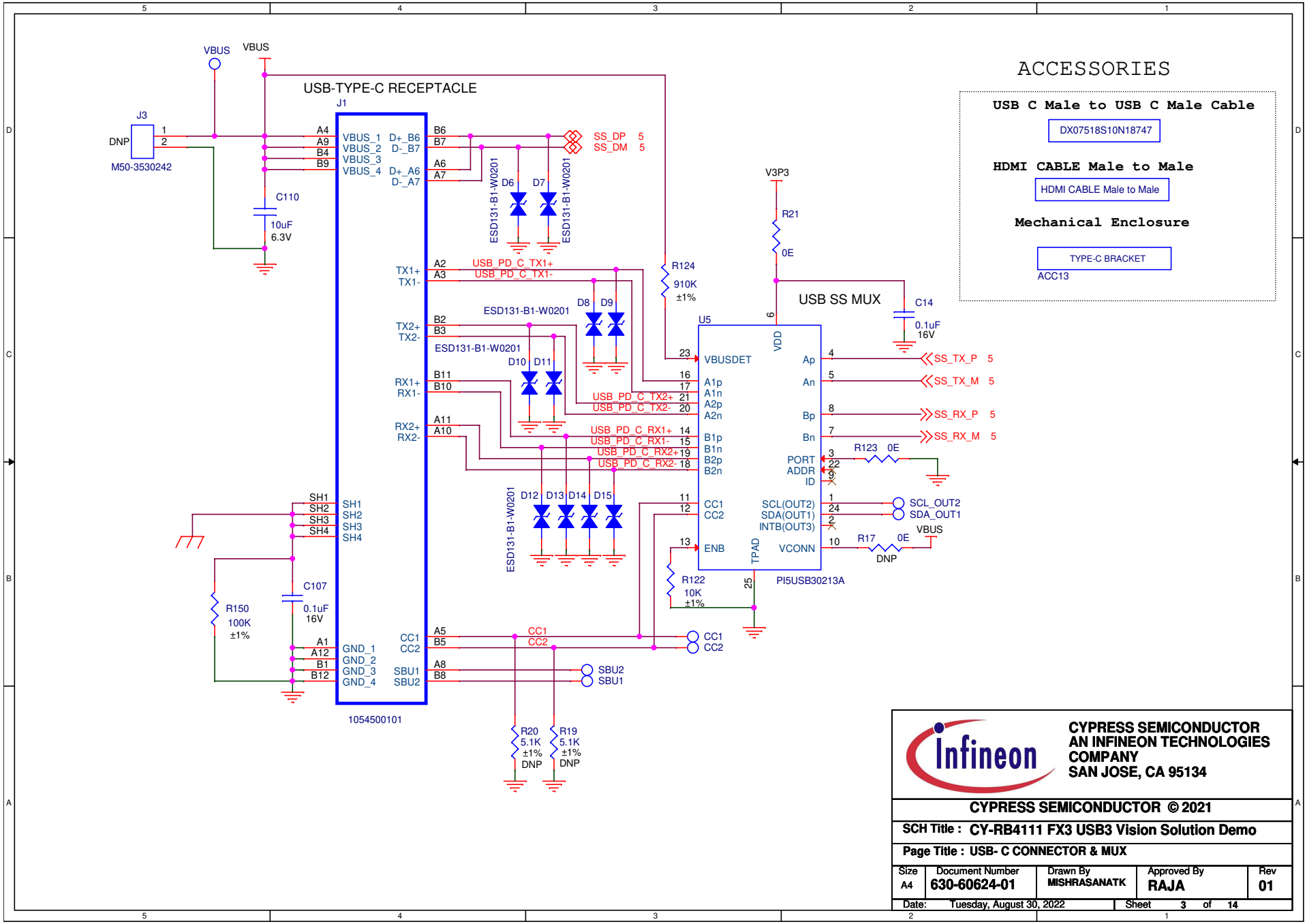

ACCESSORIES

USB C Male to USB C Male Cable

DX07518S10N18747

HDMI CABLE Male to Male

HDMI CABLE Male to Male

Mechanical Enclosure

TYPE-C BRACKET

ACC13

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Page Title : USB- C CONNECTOR & MUX				
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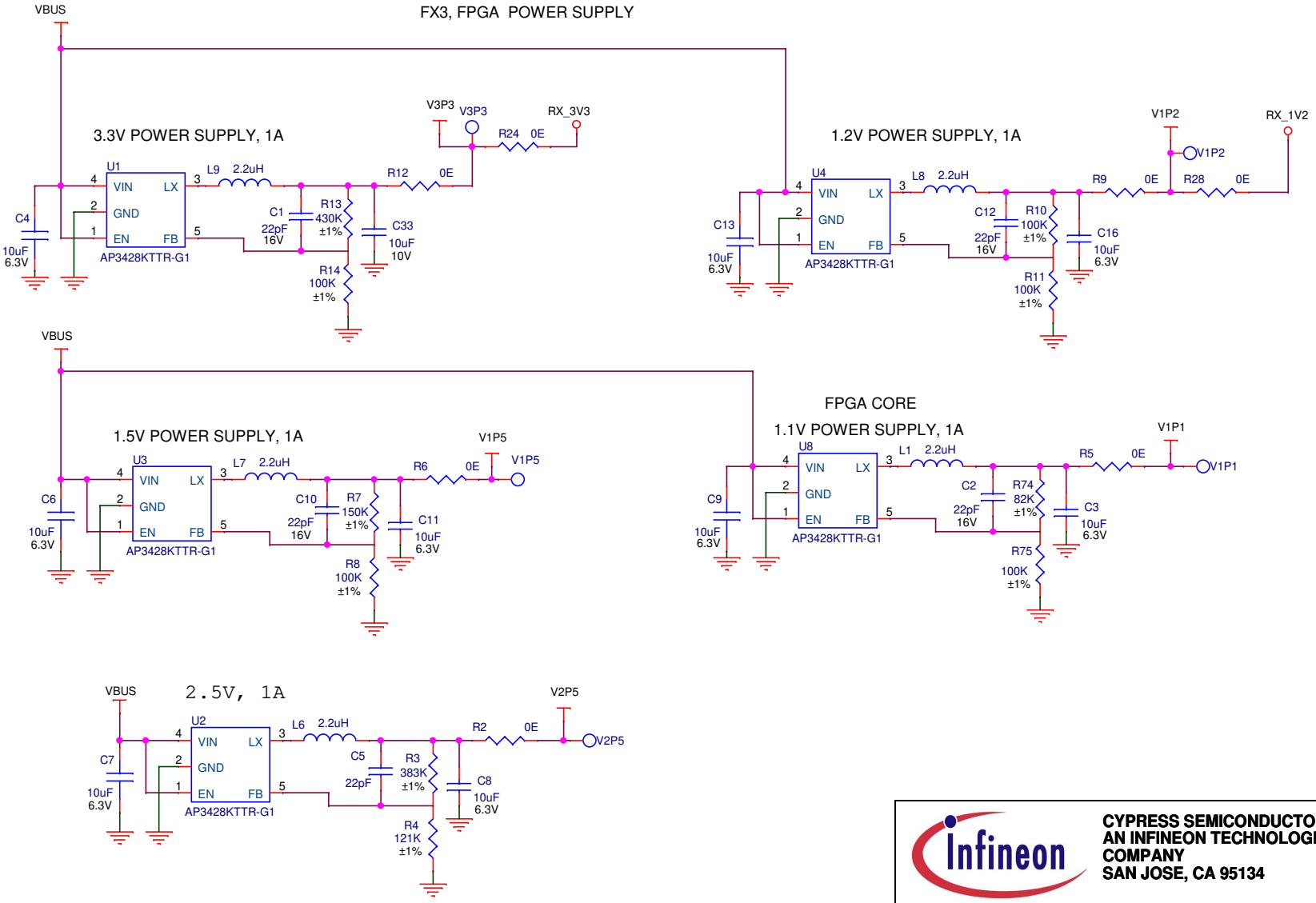
FX3, FPGA POWER SUPPLY



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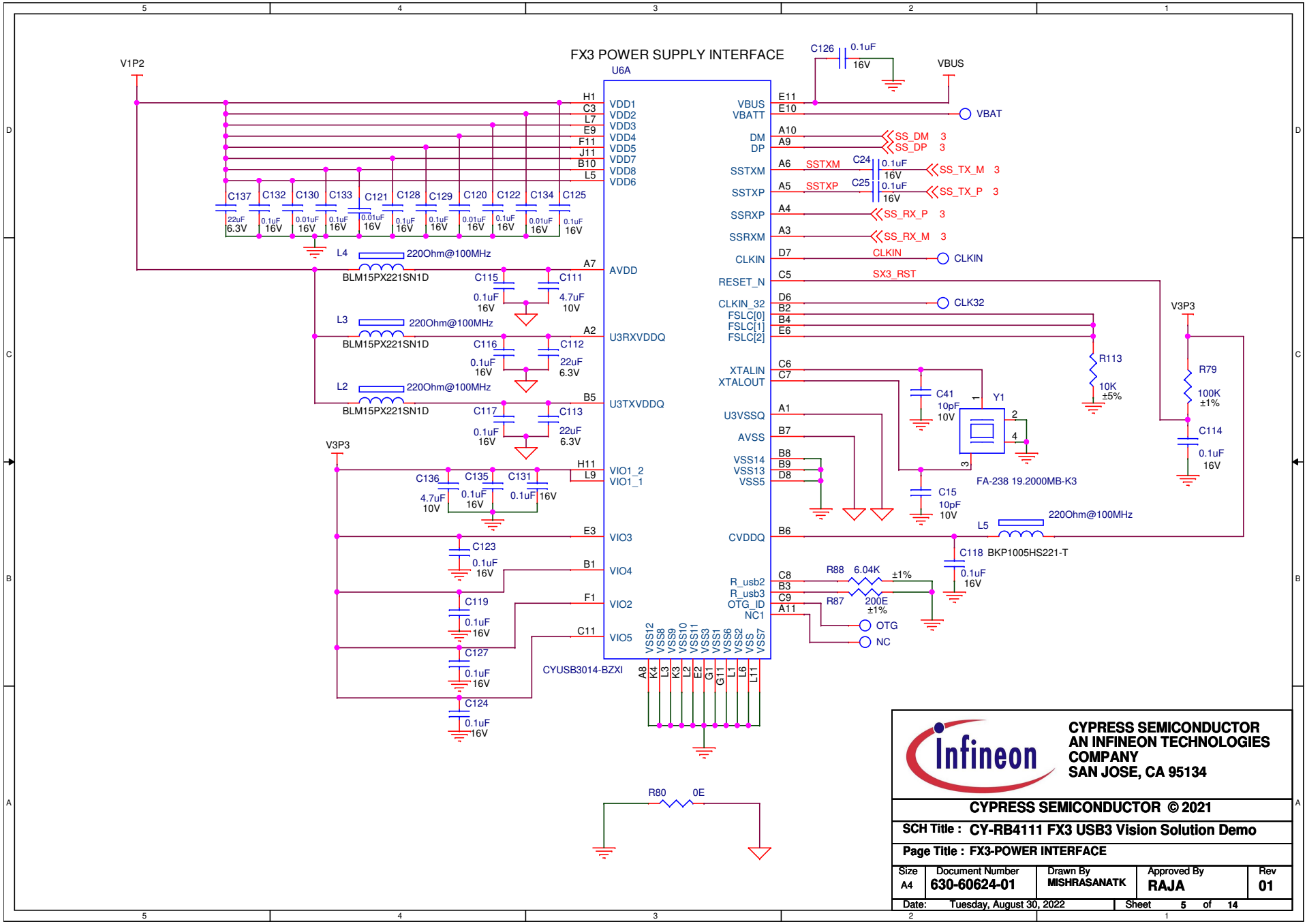

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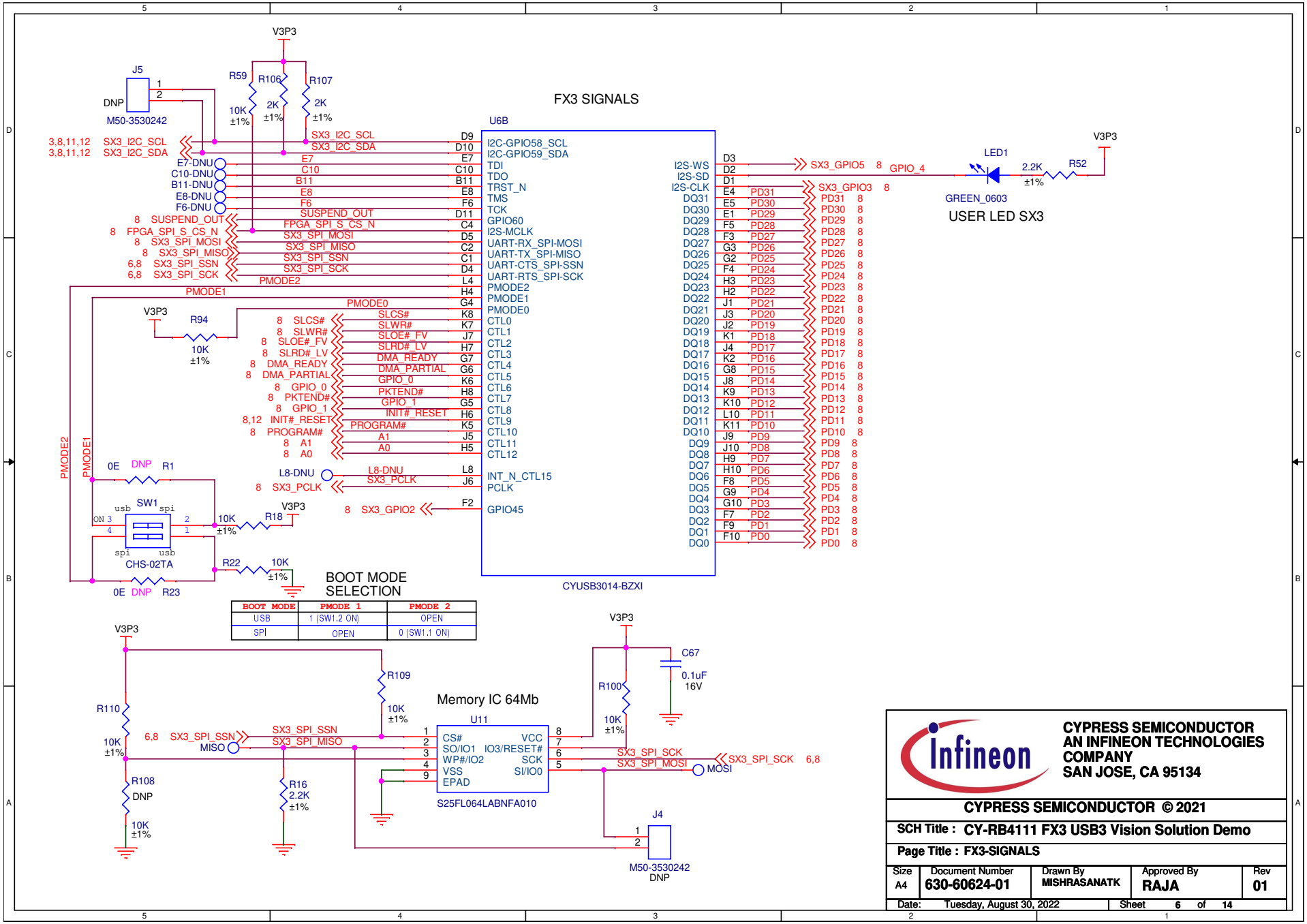

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Page Title : FX3-SIGNALS

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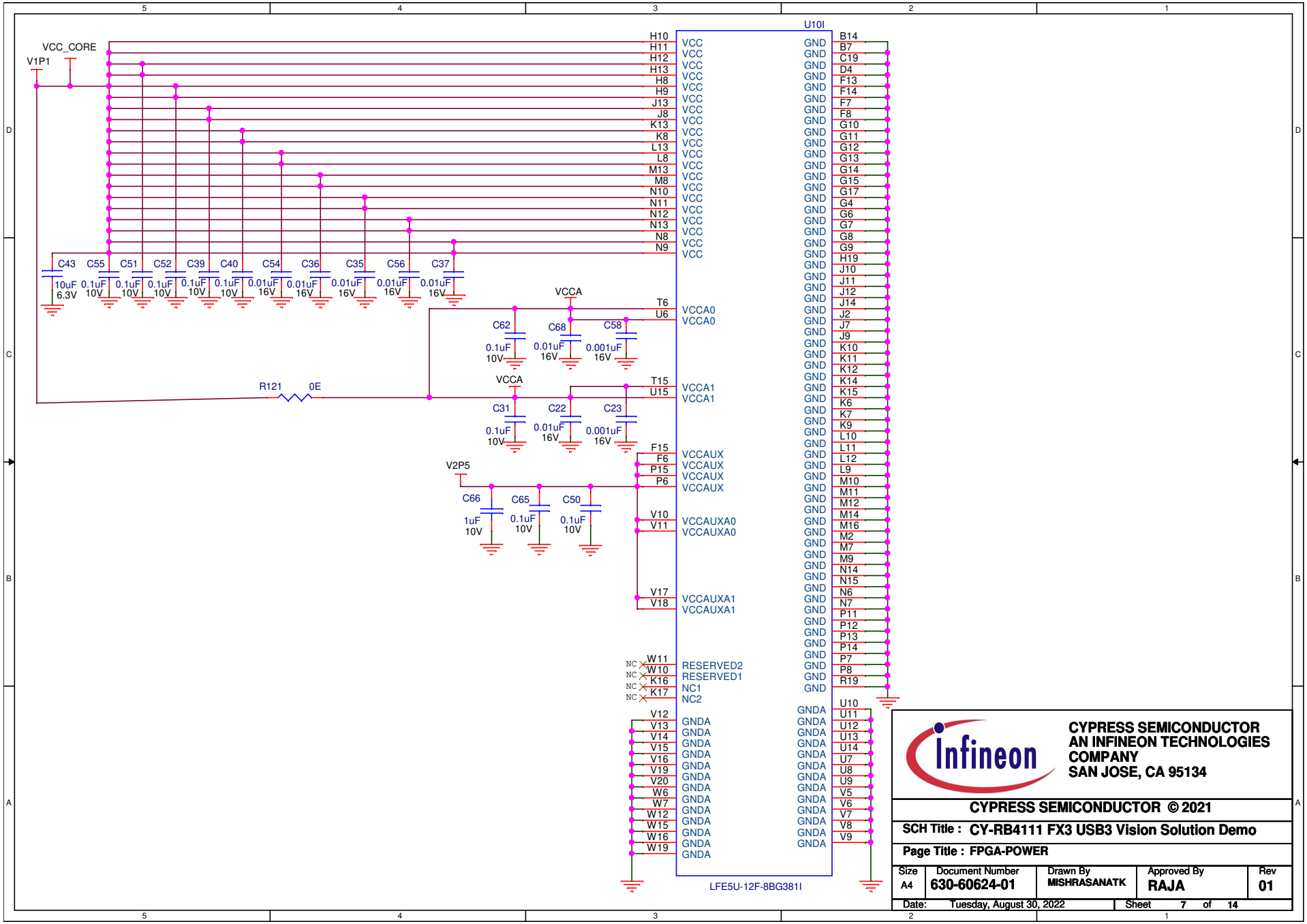
VCC_CORE
V1P1
U10I
VCC
GND
GNDA
VCCA0
VCCA1
VCCAUX
VCCAUXA0
VCCAUXA1
RESERVED2
RESERVED1
NC1
NC2
C43 10uF 6.3V
C55 C51 C52 C39 C40 0.1uF 10V
C54 C36 C35 C56 C37 0.01uF 16V
C62 0.1uF 10V
C68 0.01uF 16V
C58 0.001uF 16V
C31 0.1uF 10V
C22 0.01uF 16V
C23 0.001uF 16V
C66 1uF 10V
C65 C50 0.1uF 10V
R121 0E
VCCA
V2P5
LFE5U-12F-8BG381I
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Drawn By MISHRASANATK
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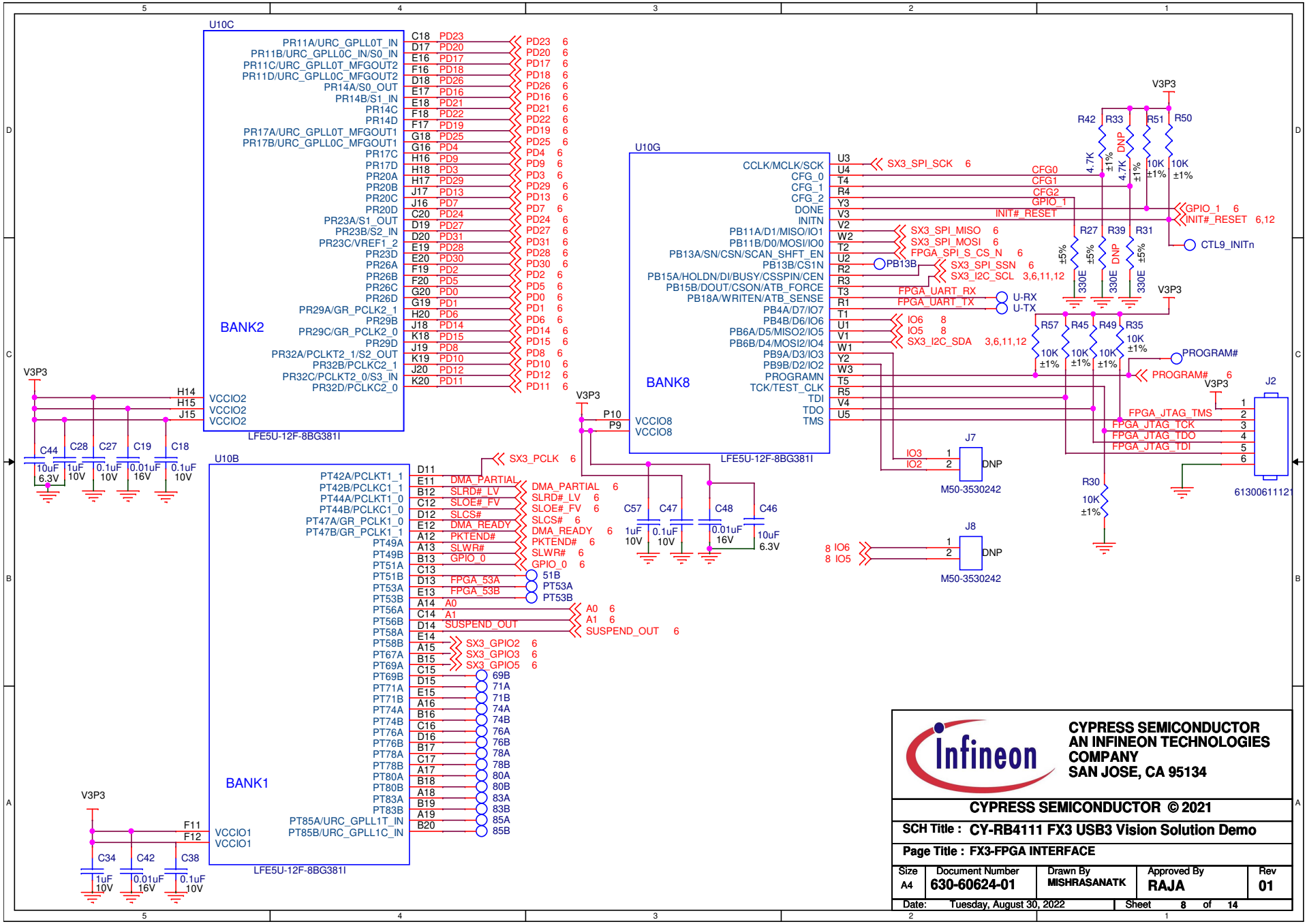
Rev 01
Date: Tuesday, August 30, 2022
Sheet 7 of 14



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Page Title : FX3-FPGA INTERFACE

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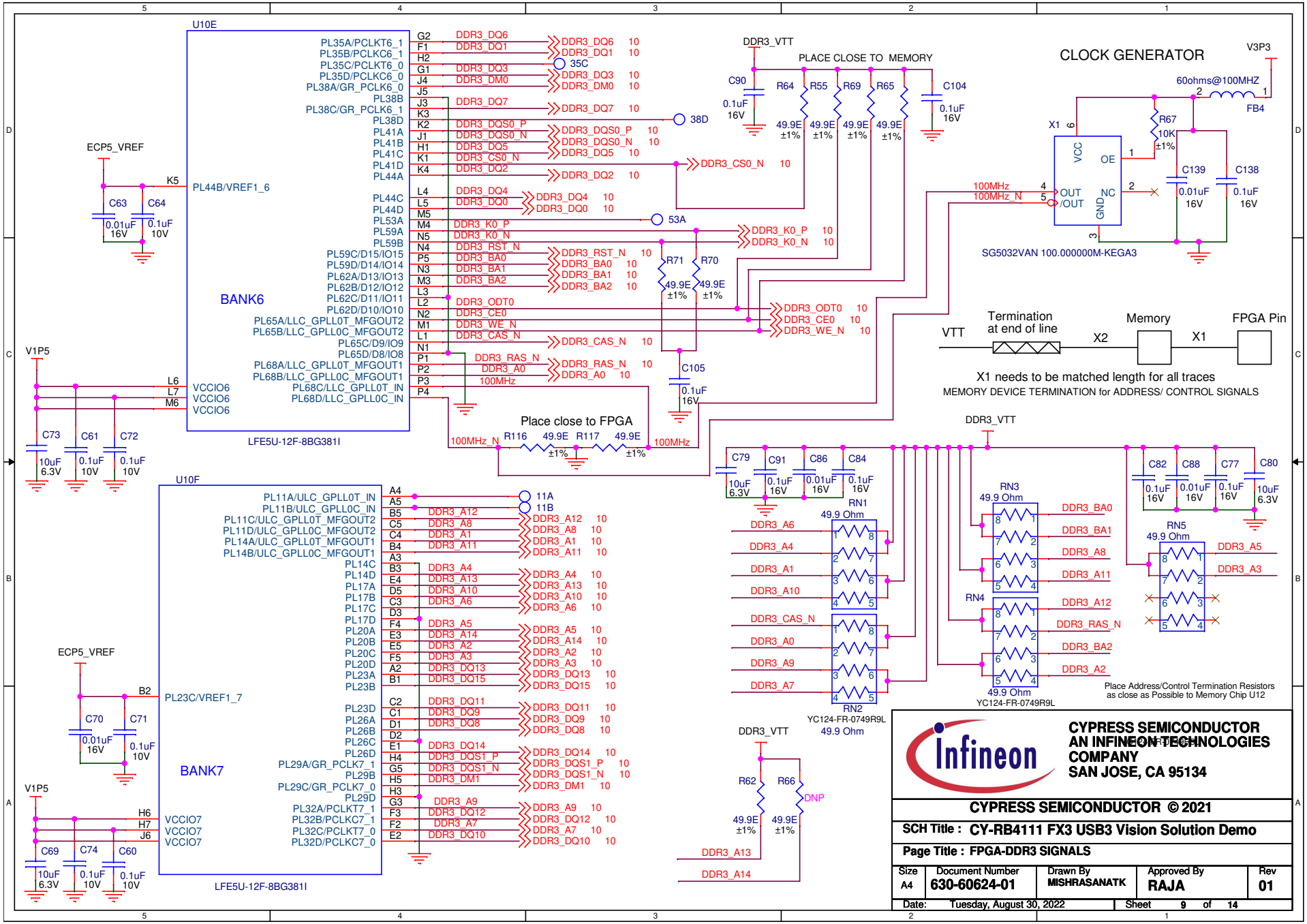
Date: Tuesday, August 30, 2022 Sheet 8 of 14


U10E
BANK6
LFE5U-12F-8BG381I
U10F
BANK7
LFE5U-12F-8BG381I
ECP5_VREF
V1P5
DDR3_VTT
PLACE CLOSE TO MEMORY
CLOCK GENERATOR
V3P3
60ohms@100MHZ
FB4
SG5032VAN 100.000000M-KEGA3
100MHz
100MHz_N
Termination at end of line
VTT
Memory
FPGA Pin
X1
X2
X1 needs to be matched length for all traces
MEMORY DEVICE TERMINATION for ADDRESS/ CONTROL SIGNALS
Place close to FPGA
Place Address/Control Termination Resistors as close as Possible to Memory Chip U12
RN1
RN2
RN3
RN4
RN5
49.9 Ohm
YC124-FR-0749R9L
DNP
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Rev 01
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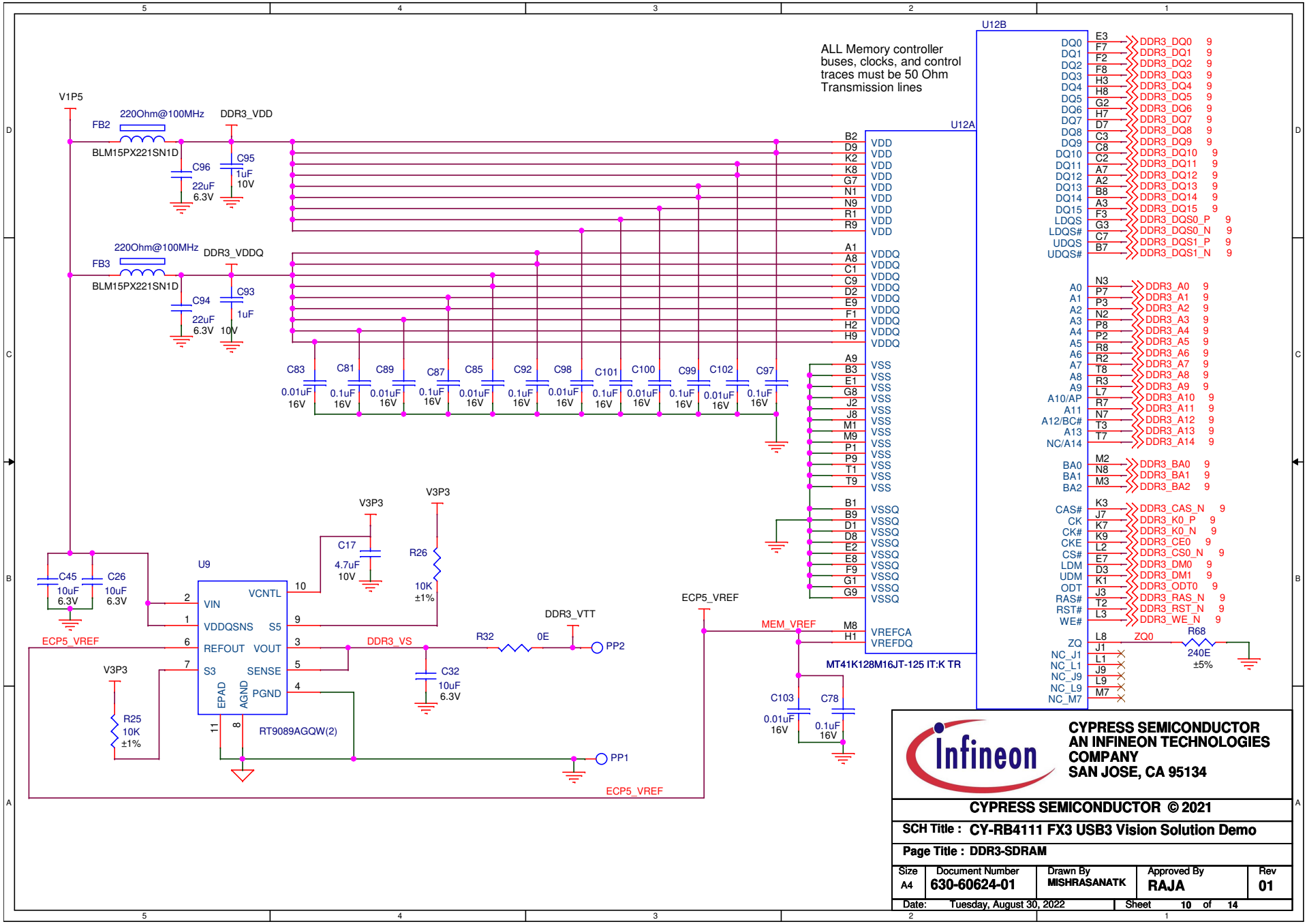
Sheet 9 of 14


ALL Memory controller buses, clocks, and control traces must be 50 Ohm Transmission lines
V1P5
FB2
220Ohm@100MHz
BLM15PX221SN1D
DDR3_VDD
C96
22uF
6.3V
C95
1uF
10V
FB3
220Ohm@100MHz
BLM15PX221SN1D
DDR3_VDDQ
C94
22uF
6.3V
C93
1uF
10V
U12A
VDD
VDDQ
VSS
VSSQ
C83 C81 C89 C87 C85 C92 C98 C101 C100 C99 C102 C97
0.01uF 0.1uF 16V
U12B
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
LDQS LDQS# UDQS UDQS#
DDR3_DQ0 DDR3_DQ1 DDR3_DQ2 DDR3_DQ3 DDR3_DQ4 DDR3_DQ5 DDR3_DQ6 DDR3_DQ7 DDR3_DQ8 DDR3_DQ9 DDR3_DQ10 DDR3_DQ11 DDR3_DQ12 DDR3_DQ13 DDR3_DQ14 DDR3_DQ15
DDR3_DQS0_P DDR3_DQS0_N DDR3_DQS1_P DDR3_DQS1_N
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 NC/A14
DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14
BA0 BA1 BA2
DDR3_BA0 DDR3_BA1 DDR3_BA2
CAS# CK CK# CKE CS# LDM UDM ODT RAS# RST# WE#
DDR3_CAS_N DDR3_K0_P DDR3_K0_N DDR3_CE0 DDR3_CS0_N DDR3_DM0 DDR3_DM1 DDR3_ODT0 DDR3_RAS_N DDR3_RST_N DDR3_WE_N
ZQ NC_J1 NC_L1 NC_J9 NC_L9 NC_M7
ZQ0
R68
240E
±5%
VREFCA VREFDQ
MEM_VREF
ECP5_VREF
MT41K128M16JT-125 IT:K TR
C103 0.01uF 16V
C78 0.1uF 16V
U9
VIN VDDQSNS REFOUT S3 VCNTL S5 VOUT SENSE PGND EPAD AGND
RT9089AGQW(2)
C45 10uF 6.3V
C26 10uF 6.3V
C17 4.7uF 10V
R26 10K ±1%
R25 10K ±1%
V3P3
DDR3_VS
R32 0E
DDR3_VTT
C32 10uF 6.3V
PP1
PP2
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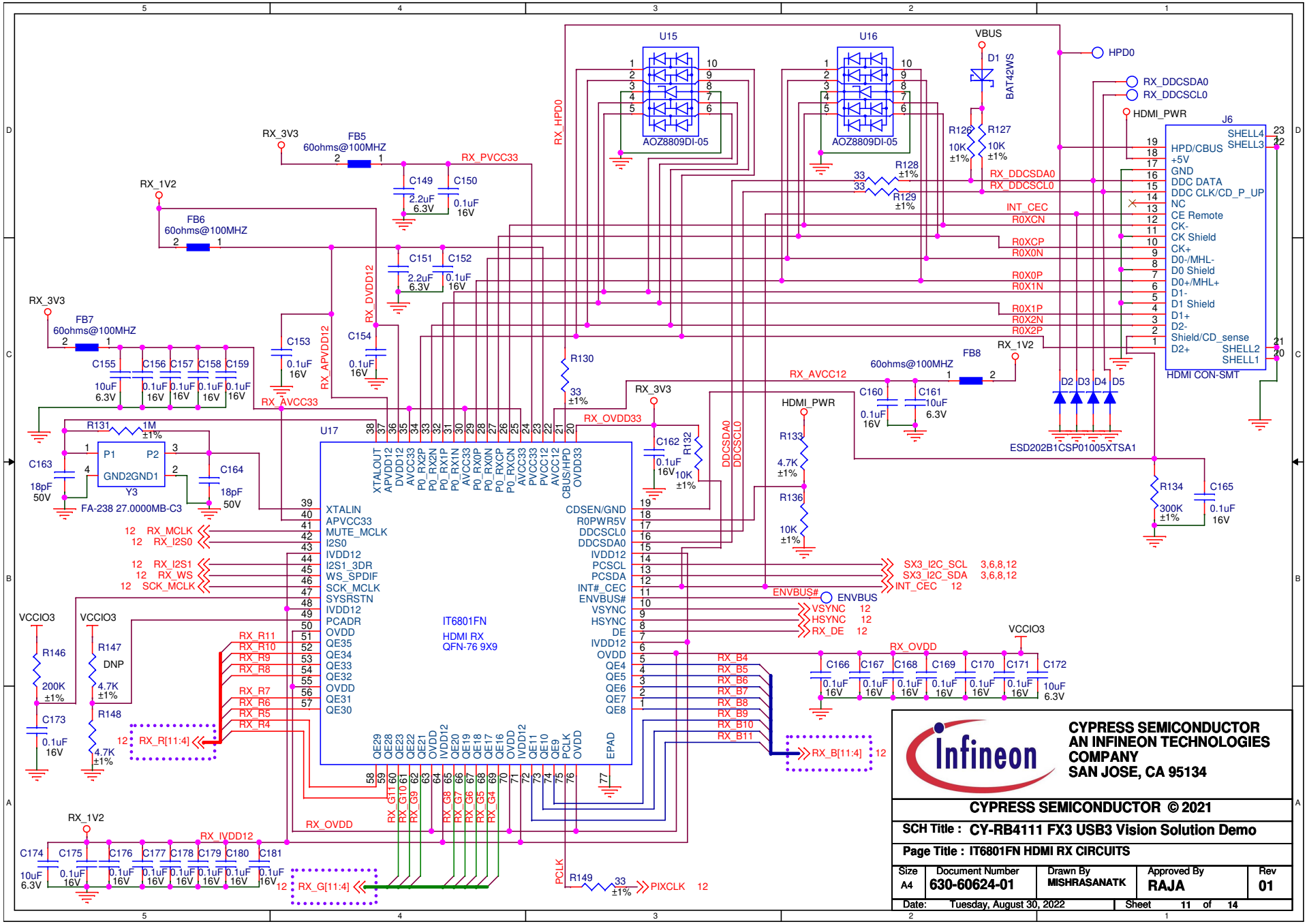
Sheet 10 of 14



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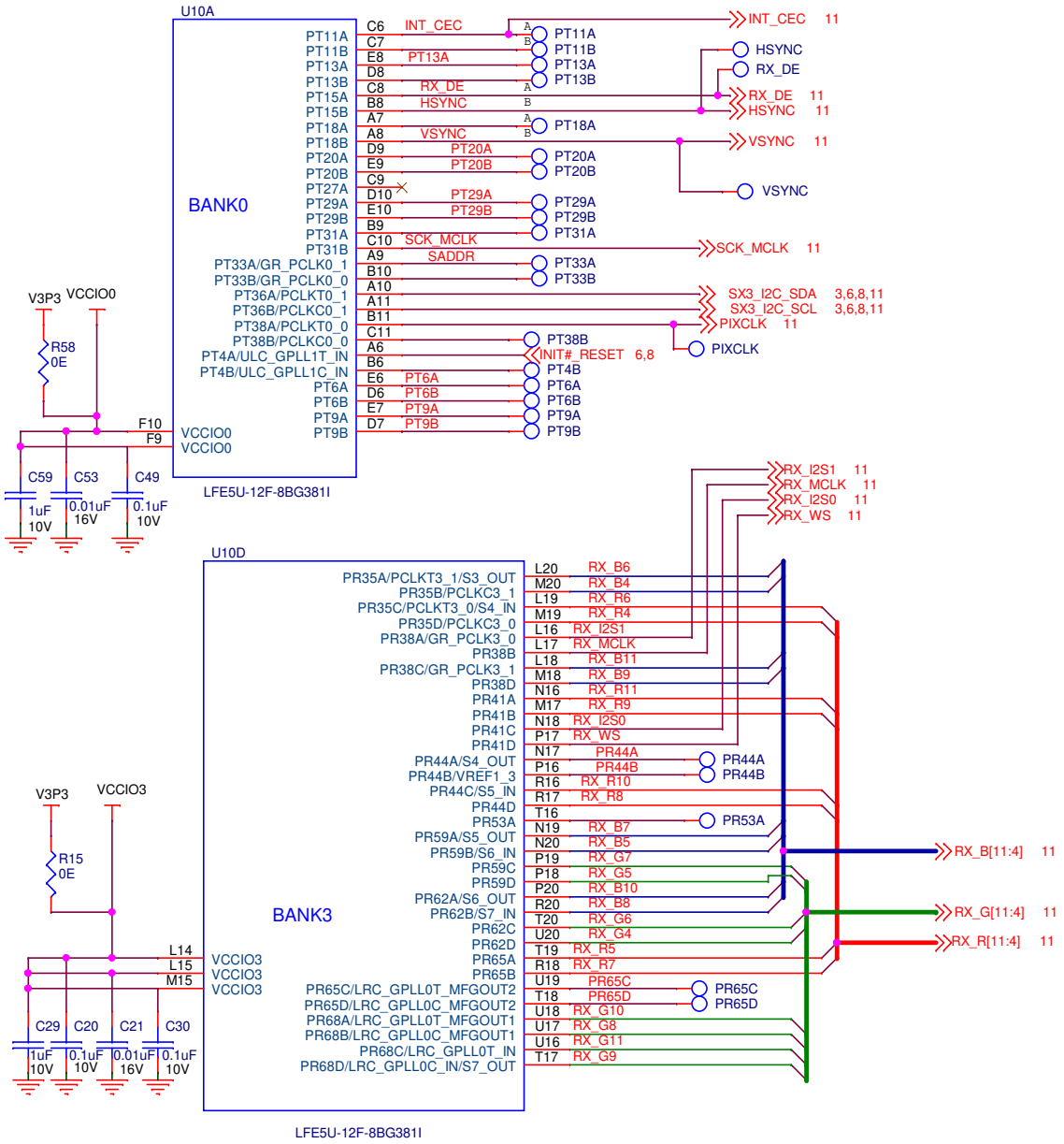
Date: Tuesday, August 30, 2022		Sheet 11 of 14		

FPGA INTERFACE



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Rev: 01	
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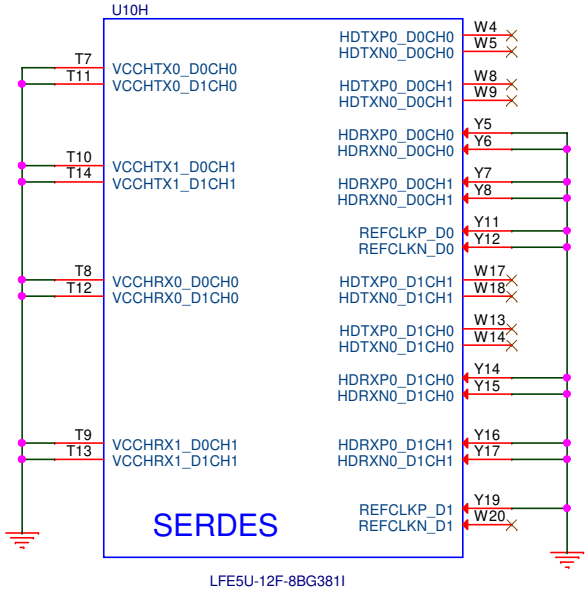

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Release	29/AUG/2022

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Date: Tuesday, August 30, 2022 Sheet 14 of 14